In the Claims

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Original) A method for controlling the performance of self testing and extended self testing, the method performed by a system that includes a first self test process and a second self test process, the method performed by the system, the method comprising:

performing the first self test process in response to a first actuation of a test control by a user of the system;

performing the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time; and

terminating the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time.

2. (Original) The method of claim 1 wherein the test control provides a one-bit binary signal having an actuated state and a non-actuated state.

3. (Original) The method of claim 1 further comprising advancing a presentation of test information in response to a fourth actuation of the test control by the user of the system during performance of the second self test process, wherein the fourth actuation is maintained for less than the second predefined period of time.

4. (Original) The method of claim 1 wherein the first self test process performs legacy functions of the system and the second self test process performs extended functions of the system.

5. (Previously Presented) A computer readable storage medium comprising computer readable instructions stored thereon to be executed by a processor, the instructions for performing the method of claim 1.

6-9. (Canceled).

10. (Original) A system comprising:

a first processor that performs a first self test process in response to a first actuation of a provided test control by a user of the system; and

a second processor that performs the second self test process in response to a second actuation of the test control prior to lapse of a first predefined period of time and terminates the second self test process in response to a third actuation of the test control by the user of the system, wherein the third actuation is maintained for more than a second predetermined period of time.

11. (Original) The system of claim 10 wherein the test control provides a one-bit binary signal having an actuated state and a non-actuated state.

12. (Original) The system of claim 10 further comprising means for advancing a presentation of test information in response to a fourth actuation of the test control by the user of the system during performance of the second self test process, wherein the fourth actuation is maintained for less than the second predefined period of time.

13. (Original) The system of claim 10 wherein the first processor further performs legacy functions of the system.

14. (Original) The system of claim 10 wherein the first processor performs a traffic collision avoidance function and the second processor performs a terrain collision avoidance function.